AMENDMENTS TO THE CLAIMS

In the Claims

The following is a marked-up version of the claims with the language that is underlined ("___") being added and the language that contains strikethrough ("—") being deleted:

1. (Original) A method for fabricating an integrated circuit device comprising:

providing a stack of semiconductor materials overlying a substrate;

depositing a stress-balancing dielectric layer overlying said stack;

depositing an anti-reflective coating (ARC) layer overlying said stress-balancing layer;

thereafter patterning said stack to form first semiconductor device structures; and

performing thermal processes to form second semiconductor device structures overlying said first semiconductor device structures wherein said stress-balancing layer prevents formation of stress-induced voids during said thermal processes.

2. (Original) The method according to Claim 1 wherein said step of providing said stack of semiconductor materials comprises:

providing shallow trench isolation regions within said substrate;

etching trenches into said shallow trench isolation regions where capacitors are to be formed;

depositing a first conducting layer into said trenches and etching away said first conducting layer except where it lines said trenches to form bottom electrodes of said capacitors;

depositing a capacitor dielectric layer overlying said bottom electrodes; and

depositing a top electrode layer overlying said capacitor dielectric layer.

3. (Original) The method according to Claim 1 wherein said balancing dielectric layer has a stress opposite to said ARC layer's intrinsic stress.

4. (Original) The method according to Claim 1 wherein said balancing dielectric layer comprises oxide, silicon nitride, or silicon oxynitride.

5. (Original) The method according to Claim 1 wherein said ARC layer comprises silicon oxynitride deposited by plasma enhanced chemical vapor deposition (PECVD).

6. (Original) The method according to Claim 1 wherein said ARC layer has an intrinsic tensile stress and wherein said stress-balancing layer has a compressive stress.

7. (Original) The method according to Claim 1 wherein said ARC layer has an intrinsic compressive stress and wherein said stress-balancing layer has a tensile stress.

8. (Original) The method according to Claim 1 wherein said first semiconductor devices are capacitors and wherein said second semiconductor devices are gate transistors.

9. (Original) The method according to Claim 1 wherein said thermal processes comprise:

growing a gate oxide layer on said substrate; and

annealing to drive in source and drain implantations.

10. (Original) The method according to Claim 1 wherein said integrated circuit comprises a single transistor SRAM device.

11. (Original) A method for fabricating an integrated circuit device comprising:

providing a stack of semiconductor materials overlying a substrate;

depositing a stress-balancing dielectric layer overlying said stack wherein said stress-balancing layer has a compressive stress;

depositing an anti-reflective coating (ARC) layer overlying said stress-balancing layer wherein said ARC layer has an intrinsic tensile stress;

thereafter patterning said stack to form first semiconductor device structures; and

performing thermal processes to form second semiconductor device structures overlying said first semiconductor device structures wherein said stress-balancing layer prevents formation of stress-induced voids during said thermal processes.

12. (Original) The method according to Claim 11 wherein said step of providing said stack of semiconductor materials comprises:

providing shallow trench isolation regions within said substrate;

etching trenches into said shallow trench isolation regions where capacitors are to be formed;

depositing a first conducting layer into said trenches and etching away said first conducting layer except where it lines said trenches to form bottom electrodes of said capacitors;

depositing a capacitor dielectric layer overlying said bottom electrodes; and

depositing a top electrode layer overlying said capacitor dielectric layer.

13. (Original) The method according to Claim 11 wherein said balancing dielectric layer comprises oxide, silicon nitride, or silicon oxynitride.

14. (Original) The method according to Claim 11 wherein said ARC layer comprises silicon oxynitride deposited by plasma enhanced chemical vapor deposition (PECVD).

15. (Original) The method according to Claim 11 wherein said first semiconductor devices are capacitors and wherein said second semiconductor devices are gate transistors.

16. (Original) The method according to Claim 11 wherein said thermal processes comprise:

growing a gate oxide layer on said substrate; and

annealing to drive in source and drain implantations.

17. (Original) The method according to Claim 11 wherein said integrated circuit comprises a single transistor SRAM device.

18. (Withdrawn) An integrated circuit device comprising:

a bottom electrode of a capacitor formed lining trenches within shallow trench isolation regions within a substrate;

a capacitor dielectric layer overlying said bottom electrode;

a top electrode layer overlying the capacitor dielectric layer within and overlying said shallow isolation regions;

a stress-balancing dielectric layer overlying said top electrode of said capacitor;

an anti-reflective coating (ARC) layer overlying said stress-balancing layer;

a gate oxide layer overlying said substrate; and

transistor gates overlying said gate oxide layer and said ARC layer over said capacitor.

19. (Withdrawn) The device according to Claim 18 wherein said stress-balancing dielectric layer has a stress opposite to said ARC layer's intrinsic stress.

20. (Withdrawn) The device according to Claim 18 wherein said stress-balancing dielectric layer comprises oxide, silicon nitride, or silicon oxynitride.

21. (Withdrawn) The device according to Claim 18 wherein said ARC layer comprises silicon oxynitride deposited by plasma-enhanced chemical vapor deposition (PECVD).

22. (Withdrawn) The device according to Claim 18 wherein said ARC layer has an intrinsic tensile stress and wherein said stress-balancing layer has a compressive stress.

23. (Withdrawn) The device according to Claim 18 wherein said ARC layer has an intrinsic compressive stress and wherein said stress-balancing layer has a tensile stress.

24. (Withdrawn) The device according to Claim 18 wherein said device comprises a single transistor RAM device.

25. (Withdrawn) The device according to Claim 18 wherein said device comprises a single transistor SRAM device.